11-16-00

A

Attorney Docket No.: 00CON159P

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

The Hon. Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Sir/Madam:

This is a request for filing a

__xx__ Continuation application ____ Divisional application

under 37 CFR 1.53(b), of pending prior application Serial No. 09/252,851

filed on: February 17, 1999 for Applicant: Hassan S. Hashemi

entitled: "Leadless Chip Carrier Design and Structure"

__XX__ 1. The filing fee is calculated below:

Claims	For	Number Filed	Number Extra	Rate	Calculations
	Total Claims	49 - 20 =	29	x $18 =	$522.00
	Indep. Claims	3 - 3 =	0	x $80 =	$ 0
	Multiple Dependent Claims			+ $270	
				Basic Fee	+ $710.00
				Total of Above =	$
	Reduction by 50% for filing by small entity				
				TOTAL =	$1,232.00

__XX__ 2. Check No. __1730__ in the amount of $__1,232.00__ is enclosed for the filing fee.

___ 3. Check No. ____ in the amount of $___ is enclosed as a petition fee for a _____ month extension of time pursuant to Rule 1.17.

XX 4. Please cancel in this application original claims 1-17 of the prior application before calculating the filing fee.

XX 5. Please amend the Specification by inserting after the title, the sentence: --This is a continuation of pending U.S. application Serial No. 09/252,851 filed February 17, 1999.--

___ 6. A verified statement to establish small entity status under 37 CFR 1.9 and 1.27 was filed in the pending prior application and such status is still proper and desired.

XX 7. The prior application is assigned of record to: Conexant Systems, Inc.

XX 8. The Power of Attorney in the present application is to:

Michael Farjami, Esq.
Farjami & Farjami LLP
16148 Sand Canyon
Irvine, California 92618
(949) 784-4600

___ (a) The Power appears in the original papers of the prior application.

XX (b) Since the Power does not appear in the original papers, a copy of the Power in the present application is enclosed.

XX (c) Recognize as associate attorney and address all future communications to:

Michael Farjami, Esq.
Farjami & Farjami LLP
16148 Sand Canyon
Irvine, California 92618
(949) 784-4600

XX 9. A preliminary amendment is enclosed.

XX 10. It is hereby requested that any request for a convention priority made in the prior application be transferred to this Rule 1.53(b) application.

___ 11. Applicant hereby petitions for an extension of time pursuant to Rule 1.136, if one is needed, for the above-noted prior application. A duplicate copy of this sheet is enclosed for filing in the proper application file.

XX 12. Enclosed is a copy of the latest inventor-signed application, including a copy of the oath or declaration as originally filed. I hereby verify that the papers are a true copy of the latest signed application Serial No. 09/252,851 , as filed on February 17,

1999. No amendments referred to in the oath or declaration filed to complete the latest signed application, or the continuation thereof, introduced new matter therein.

XX 13. The pending parent application Serial No. 09/252,851 has received a Notice of Allowance and is in Class 257, Subclass 706.000 in Art Unit 2815.

XX 14. The Commissioner is hereby authorized to charge payment of any additional fees associated with this communication, or credit any overpayment, to Deposit Account Number 50-0731. A duplicate of this authorization is enclosed.

The undersigned declares further, that all statements made herein of his own knowledge are true, and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Respectfully submitted,

Date: 11/15/00

MICHAEL FARJAMI
Reg. No. 38,135

___ Inventor(s)
___ Assignee of Complete Interest
XX Attorney of Record in the Present Application.

Michael Farjami, Esq.
Farjami & Farjami LLP
16148 Sand Canyon
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Date of Deposit 11-15-2000
I hereby certify that this paper is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. §1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231, on

Sara Ansari
(Signature)

Sara Ansari
(Typed or Printed Name of Person Mailing Paper or Fee)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: Hassan S. Hashemi	
Serial No.:	Examiner:
Filed:	Group Art Unit:
For: Leadless Chip Carrier Design and Structure	
This is a Rule 1.53(b) continuation of pending U.S. Application Serial No. 09/252,851 filed February 17, 1999 and assigned to the assignee of the present application.	

PRELIMINARY AMENDMENT TO CONTINUATION APPLICATION

Honorable Commissioner of
Patents and Trademarks
Washington, D. C. 20231

Dear Sir/Madam:

This amendment is directed to the accompanying 37 CFR §1.53(b) continuation application. The parent application Serial No. 09/252,851, filed February 17, 1999 has received a Notice of Allowance and is in Class 257, Subclass 706.000 in Art Unit 2815. Please enter the following amendments in the present §1.53(b) continuation application.

In the Specification:

After the title, please insert the sentence: --This is a continuation of application Serial No. 09/252,851 filed February 17, 1999.--

On page 6, line 25, please replace "vias 260" with --vias 250--.

In the Claims:

Please cancel claims 1-17.

Please add the following new claims:

--18. A structure comprising:

a substrate having a top surface for receiving a chip;

a printed circuit board attached to a bottom surface of said substrate;

at least one via in said substrate;

said at least one via providing an electrical connection between a device electrode of said chip and said printed circuit board.--

--19. The structure of claim 18 wherein said chip is a semiconductor chip.--

--20. The structure of claim 18 wherein said substrate comprises organic material.--

--21. The structure of claim 20 wherein said organic material is selected from the group consisting of polytetrafluoroethylene material and an FR4 based laminate material.--

--22. The structure of claim 18 wherein said substrate comprises a ceramic material.--

--23. The structure of claim 18 wherein said at least one via provides an electrical connection between a bond pad and said printed circuit board, wherein said bond pad is electrically connected to said device electrode.--

--24. The structure of claim 23 wherein said at least one via abuts said bond pad.--

--25. The structure of claim 23 wherein said bond pad is electrically connected to said device electrode by a bonding wire.--

--26. The structure of claim 18 wherein said at least one via provides an electrical connection between said device electrode and a land, said land being electrically connected to said printed circuit board.--

--27. The structure of claim 26 wherein said at least one via abuts said land.--

--28. The structure of claim 18 wherein said at least one via provides an electrical connection between a bond pad and a land, wherein said bond pad is electrically connected to said device electrode, and wherein said land is electrically connected to said printed circuit board.--

--29. The structure of claim 28 wherein said at least one via abuts said bond pad and said land.--

--30. The structure of claim 28 wherein said bond pad is electrically connected to said device electrode by a bonding wire.--

--31. The structure of claim 29 wherein said bond pad is electrically connected to said device electrode by a bonding wire.--

--32. The structure of claim 18 wherein said at least one via comprises copper.--

--33. The structure of claim 18 wherein said at least one via comprises a thermally conductive material.--

--34. A structure comprising:

a substrate having a top surface and a bottom surface;

a semiconductor chip attached to said top surface of said substrate;

a heat spreader attached to said bottom surface of said substrate;

a first via in said substrate;

said first via providing a connection between said semiconductor chip and said heat spreader.--

--35. The structure of claim 34 wherein said heat spreader is attached to a printed circuit board.--

--36. The structure of claim 34 wherein said heat spreader is an electrical conductor.--

--37. The structure of claim 36 wherein said heat spreader is attached to a printed circuit board by solder.--

--38. The structure of claim 34 wherein said heat spreader is a thermal conductor.--

--39. The structure of claim 38 wherein said heat spreader is attached to a printed circuit board by solder.--

--40. The structure of claim 34 wherein a second via in said substrate provides a connection between a device electrode of said semiconductor chip and a printed circuit board.--

--41. The structure of claim 34 wherein said first via provides an electrical connection between said semiconductor chip and said heat spreader.--

--42. The structure of claim 40 wherein said first via provides an electrical connection between said semiconductor chip and said heat spreader.--

--43. The structure of claim 34 wherein said first via provides a thermal connection between said semiconductor chip and said heat spreader.--

--44. The structure of claim 40 wherein said first via provides a thermal connection between said semiconductor chip and said heat spreader.--

--45. The structure of claim 34 wherein said substrate comprises organic material.--

--46. The structure of claim 45 wherein said organic material is selected from the group consisting of polytetrafluoroethylene material and an FR4 based laminate material. --

--47. The structure of claim 34 wherein said substrate comprises a ceramic material.--

--48. The structure of claim 40 wherein said second via provides an electrical connection between a bond pad and said printed circuit board, wherein said bond pad is electrically connected to said device electrode.--

--49. The structure of claim 48 wherein said second via abuts said bond pad.--

--50. The structure of claim 48 wherein said bond pad is electrically connected to said device electrode by a bonding wire.--

--51. The structure of claim 40 wherein said second via provides an electrical connection between said device electrode and a land, said land being electrically connected to said printed circuit board.--

--52. The structure of claim 51 wherein said second via abuts said land.--

--53. The structure of claim 40 wherein said second via provides an electrical connection between a bond pad and a land, wherein said bond pad is electrically connected to said device electrode, and wherein said land is electrically connected to said printed circuit board.--

--54. The structure of claim 53 wherein said second via abuts said bond pad and said land.--

--55. The structure of claim 53 wherein said bond pad is electrically connected to said device electrode by a bonding wire.--

--56. The structure of claim 34 wherein said first via comprises copper.--

--57. The structure of claim 40 wherein said second via comprises copper.--

--58. A structure comprising:

a substrate having a top surface and a bottom surface;

a semiconductor chip attached to said top surface of said substrate;

a heat spreader attached to said bottom surface of said substrate;

a first plurality of vias in said substrate;

said first plurality of vias providing a connection between said semiconductor chip and said heat spreader.--

--59. The structure of claim 58 wherein said heat spreader is attached to a printed circuit board.--

--60. The structure of claim 59 wherein a second plurality of vias in said substrate provide connections between a plurality of device electrodes of said semiconductor chip and said printed circuit board.--

--61. The structure of claim 58 wherein said first plurality of vias provide an electrical connection between said semiconductor chip and said heat spreader.--

--62. The structure of claim 58 wherein said first plurality of vias provide a thermal connection between said semiconductor chip and said heat spreader.--

--63. The structure of claim 60 wherein said second plurality of vias provide electrical connections between a plurality of bond pads and said printed circuit board, wherein each of said plurality of bond pads is electrically connected to a respective one of said plurality of device electrodes.--

--64. The structure of claim 60 wherein said second plurality of vias provide electrical connections between each one of said plurality of device electrodes and a respective one of a plurality of lands, said plurality of lands being electrically connected to said printed circuit board.--

--65. The structure of claim 58 wherein said first plurality of vias comprise copper.--

--66. The structure of claim 60 wherein said second plurality of vias comprise copper.--

REMARKS

This is a Rule 1.53(b) continuation application of the parent application, Serial No. 09/252,851, filed February 17, 1999. The parent application has received a Notice of Allowance of claims 1-17 in the parent application. This continuation application is filed during the pendency of the parent application. By this preliminary amendment, applicant has canceled claims 1-17 (which were allowed in the pending parent application) and has added new claims 18-66. No new matter has been introduced in the present continuation application. Accordingly, claims 18-66 remain in the present Rule 1.53(b) continuation application. Consideration and examination of pending claims 18-66 is respectfully requested.

A true and correct copy of the parent application, including the specification, drawings and claims, as originally filed, is enclosed. Also enclosed is a true and correct copy of the declaration as filed in the parent application. Applicant has also enclosed formal drawings corresponding to the original filed drawings. It is noted that in the enclosed formal drawings, Figure 1 has been amended to include the label "Prior Art" as requested by the Examiner in the pending parent application.

Moreover, Applicant has enclosed a "Revocation and Power of Attorney" to formalize the fact that the attorneys in the present continuation application are different from the attorneys of record in the pending parent application. The Examiner is respectfully requested to take note of the "Revocation and Power of Attorney" and direct all correspondence to the undersigned attorney in the present continuation application whose address and phone number appear below.

Respectfully submitted,

Date: 11/15/00

Michael Farjami, Esq.
Reg. No. 38,135

Michael Farjami, Esq.
FARJAMI & FARJAMI LLP
16148 Sand Canyon
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Sara Ansari
(Signature)

Sara Ansari
(Typed or Printed Name of Person Mailing Paper or Fee)

UNITED STATES PATENT APPLICATION

for a new and useful invention entitled

LEADLESS CHIP CARRIER DESIGN AND STRUCTURE

by Inventor:

Hassan S. Hashemi

Conexant Docket No. 98RSS246

Snell & Wilmer, L.L.P. Docket No. 50944.2100

Leadless Chip Carrier Design and Structure

Inventor: Hassan S. Hashemi

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to electronic packaging, and more particularly, to a leadless chip carrier design and structure.

2. Description of the Related Art

The microelectronics industry has continued to make significant advances in semiconductor device technology. Semiconductor devices are getting smaller, more dense, and run at higher speeds. However, as device sizes decrease and electrical components are moved closer together, one of the limiting properties of the semiconductor device is the electrical parasitics caused by resistance, capacitance and inductance effects. This is particularly troubling in radio frequency (RF) devices, where it is important to minimize electrical parasitics and to be able to predict their effects reliably. Also, the need to control device generated heat has become more critical as the speeds and power consumption of semiconductor devices has increased.

Controlling electrical parasitics is also important at the packaging level. The structure that supports the semiconductor device (i.e., chip) is commonly referred to as an electronic package. The electronic package is designed to provide electrical interconnection for I/O, signal lines, power supplies, and ground, in addition to environmental and physical protection.

One advantageous form of packaging is the chip carrier which is gaining in popularity. A big reason for this is that chip carriers are very small in size and thus make it possible to fit many devices on a substrate such as a printed circuit board (PCB) or ceramic. The package, as part of the completed semiconductor device, must be low in electrical parasitics and have good thermal dissipation. This is especially important for RF applications.

Electrical parasitics, particularly inductance, are some of the parameters that can adversely affect the performance of electrical packages. Inductance is thus one parameter that should be controlled and reduced. One of the factors contributing to the inductance is the long printed traces found in most packages. Another factor is the lack of a good ground plane located close to the device.

Present packages also have problems with dissipating heat. As semiconductor devices have increased in performance, their power requirements have also increased dramatically. Because of the large amount of power needed to operate a chip, the heat generated by a chip can reach several watts. Dissipation of this heat is an important design consideration of both the chip and chip carrier. Since the chip and chip carrier are made from different materials, each having a different coefficient of thermal expansion, they will react differently to the heat generated by the chip and the outside environment. The resulting thermal stresses can reduce the life of the semiconductor device by causing mechanical failures. Thus, it is desirable to be able to predict accurately the thermal effects of the chip carrier so that the chip carrier can be designed accordingly.

Therefore, there exists a need for a small package for a semiconductor device that would provide low electrical parasitics, predictable heat dissipation along with an efficient ground plane.

SUMMARY OF THE INVENTION

In accordance with one embodiment of the present invention, a semiconductor device is provided in the form of a chip carrier that includes a semiconductor chip attached to the upper surface of an interconnect substrate. A die attach pad is provided on the upper surface of the interconnect substrate and the chip is attached to this pad. On the lower surface of the substrate is a heat spreader positioned beneath the die attach pad. A plurality of vias extend through the thickness of the substrate from the upper surface to the lower surface. A first group of these vias is positioned to intersect both the die attach pad and the heat spreader. A second group of these vias is positioned apart from both the die attach pad and the heat spreader. Bonding pads are positioned to abut the second group of vias on the upper surface

of the interconnect substrate. Device electrodes on the semiconductor chip are electrically coupled to these bonding pads by wire bonds. Electrically conductive lands are positioned to abut the second group of vias on the lower surface of the interconnect substrate and can be used to connect the semiconductor device to a printed circuit board or other electronic equipment.

BRIEF DESCRIPTION OF THE DRAWINGS

A preferred embodiment of the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The preferred embodiment, however, both as to organization and method of operation, may best be understood by reference to the following description taken in conjunction with the claims and the accompanying drawings, in which like parts may be referred to by like numerals:

FIG. 1 illustrates an electronic packaging hierarchy;

FIGS. 2-4 illustrate, in cross-sectional, top and bottom views, respectively, one embodiment of the invention; and

FIG. 5 illustrates, in cross-section view, a chip carrier in accordance with an alternate embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EXEMPLARY EMBODIMENTS

The present invention provides for a more efficient electronic device particularly suited for radio frequency (RF) applications by minimizing electrical parasitics and providing for predictable electrical and thermal performance. The electronic device in accordance with the invention is especially applicable to devices with up to approximately 64 leads, which is particularly suited to many RF and analog applications, but it will be readily appreciated that the following description also applies to packages of different sizes and different number of I/O pins.

Referring now to **FIG. 1**, an electronic packaging hierarchy is illustrated. A semiconductor device chip 100 is mounted on an electronic package 110 to form a semiconductor device 120. The resulting semiconductor device can be connected to a printed circuit board 130 that is plugged into a mother board (not shown).

FIG. 2 illustrates in cross-section, a semiconductor device 120 in accordance with a preferred embodiment of the present invention. Device 120 includes semiconductor device chip 100 which is preferably an integrated circuit (IC) chip. The semiconductor device also

includes an interconnect substrate 220 having an upper surface 200 and a lower surface 210. The upper and lower surface of the interconnect substrate preferably are planar. Upper surface 200 of the interconnect substrate has a die attach bond pad 240 to which semiconductor device chip 100 is attached. Die attach bond pad 240 is a metallic pad formed of a metal that is highly conductive, both electrically and thermally. In the preferred embodiment, interconnect substrate 220 suitably comprises an organic (i.e., laminate) material such as a polytetrafluoroethylene (PTFE) or FR4 based laminate. However, other alternative embodiments may use other organic or non-organic (i.e., ceramic) materials for interconnect substrate 220.

Semiconductor device chip 100 is attached to die attach bond pad 240 of interconnect substrate 220 using a conventional conductive epoxy die attach epoxy 230. For example, an epoxy such as Ablebond 84-ILMIT or Sumitomo 1079B can be used. Alternatively, solder or other well known die attach material can be used depending on the interconnect substrate material and the intended use of the device.

A heat spreader 290 is located on lower surface 210 of interconnect substrate 220. Similar to die attach bond pad 240, heat spreader 290 is a metallic pad formed of a metal that is highly conductive, both electrically and thermally. As described below, heat spreader 290 is used to both electrically and thermally connect semiconductor device 120 to a printed circuit board (PCB).

A plurality of vias passes through the thickness of interconnect substrate from upper surface 200 to lower surface 210. Each of the vias is filled with a material such as copper that is both electrically and thermally conductive. The filled vias thus provide electrical and thermal pathways from upper surface 200 to lower surface 210.

A first group of vias 255 are illustrated in **FIG. 2**. First group of vias 255 is positioned to intersect both die attach pad 240 on the upper surface and heat spreader 290 on the lower surface 210 of interconnect substrate 220. First group of vias 255 thus provides for a good thermal and electrical connection from semiconductor device chip 100 to heat spreader 290 due to the presence of an electrical and thermal conductor such as copper.

A second group of vias 250 is positioned about the periphery of and spaced away from semiconductor device chip 100 as is more clearly seen in **FIG. 3**. **FIG. 3** illustrates semiconductor device 120 in top view. In accordance with the invention, a plurality of bond pads 260 is formed on upper surface 200 of interconnect substrate abutting the second group of vias 250. The plurality of bond pads is preferably positioned in a peripheral design along the perimeter of the upper surface of the interconnect substrate. However, it will be appreciated that the plurality of bond pads may be positioned in other designs such as either a regular or irregular array of columns and rows. Whatever the design, the second group of vias 250 and the array of bond pads 260 are designed so that the vias abut the pads.

Semiconductor device chip 100 includes a plurality of device electrodes 300 on its upper surface. These device electrodes 300 provide the means by which electrical contact, including I/O, power supplies, and ground, is made to the electrical circuit contained on semiconductor device chip 100. Electrical connection must be made from device electrodes 300 to bond pads 260 of interconnect substrate 220 and ultimately to the printed circuit board and the mother board.

Referring to **FIGS. 2** and **3**, in the preferred embodiment, semiconductor device chip 100 is electrically connected to interconnect substrate 220 of the chip carrier by a technique called wire bonding. In wire bonding, the electrical connections are made by bonding wires 270, preferably very small wires, between device electrodes 300 of the semiconductor device chip 100 to bond pads 260 on interconnect substrate 220. The bond attachment is completed by thermal compression bonding or other well known wire bonding methods. Typically, wires and bond pads that are gold or gold-plated, aluminum or an alloy of aluminum, or copper or an alloy of copper are used.

In accordance with the invention, as illustrated in **FIG. 3**, each of the plurality of bond pads 260 is located immediately adjacent to or abuts one of second group of vias 260. No traces are necessary between the bond pads and the vias, so parasitic inductance is reduced. The bond pads 260 are directly coupled to the plurality of lands 280 located on the lower surface 210 of the interconnect substrate 220 by the copper or other conductive material filling the vias. The lands 280 can be connected to a signal on the PCB 130 or to a ground or power

source. It will be readily appreciated that this will reduce the electrical inductance of semiconductor device 120 as this minimizes the distance from bond pads 260 to vias 250. Thus, the flexibility of wire bonding can be utilized to pick the shortest path from semiconductor device chip 100 to bond pads 260 and the resultant inductance will be minimal. Space is saved since traces are not needed to connect bond pads 260 to vias 250. It has been found, for example, that what was previously a 9x9 mm 48 I/O package can be reduced to a 6x6 mm 48 I/O package. Therefore, the size of interconnect substrate 220 is only slightly larger than the size of semiconductor device chip 100.

Referring now to **FIG. 4**, a bottom view of semiconductor device 120 according to a preferred embodiment of the present invention is illustrated. Second group of vias 250 passes through interconnect substrate 220 and are exposed on lower surface 210. Lower surface 210 of the interconnect substrate 220 also has a plurality of lands 280 and heat spreader 290. Lower surface 210 of interconnect substrate 220 is adapted to be attached to the printed circuit board (not shown) by soldering heat spreader 290 and plurality of lands 280 to corresponding metallization on the printed circuit board. Using heat spreader 290 to attach to the printed circuit board allows for a good thermal path at a very low thermal resistance. Large heat spreader 290 also helps to increase the reliability of the bonds to the plurality of lands 280 as is explained below.

There is increased reliability because the mechanical stress or physical displacement on the plurality of lands 280, due to the heating and cooling of the semiconductor device, is decreased due to the presence of large heat spreader 290. A difference may exist in the coefficient of thermal expansion (CTE) between the semiconductor device and the PCB because they may be constructed of different materials. If so, when the semiconductor device heats up due to operating or environmental factors, there will be a physical strain on the connections (i.e., lands 280 and heat spreader 290) between the semiconductor device and the PCB to which the semiconductor device is attached. The copper exposed pad of large heat spreader 290 reduces the CTE mismatch. The large exposed pad of heat spreader 290 more than compensates for the 4-6 mil nominal solder stand-off between the semiconductor device

and the PCB. Heat spreader 290 dominates the overall solder joint strain, thus increasing the physical reliability of lands 280.

Electrical inductance is also reduced by the presence of downbonds as is explained next. In addition to electrical contact between the back side of semiconductor device chip 100 to die attach bond pad 240, additional connections can be made from preselected device electrodes 300 as needed, by down bonding from semiconductor device chip 100 to die attach bond pad 240. Referring back to **FIG. 2**, downbonds 295 allow the preselected device electrodes of the semiconductor device chip to be electrically connected to die attach bond pad 240 and to heat spreader 290 by way of the first group of vias 255. Using downbonds 295 will also lead to minimal inductance because the length of wire used is minimal, and it thus provides for a very good electrical and thermal path from semiconductor device chip 100 to the ground plane.

The semiconductor device just described is compatible with a simple manufacturing process that comprises overmolding a plurality of devices in a panelization scheme, and then sawing the overmolded devices into single devices at the end of the manufacturing process. This allows for the semiconductor device of the present invention to make use of portions of existing manufacturing processes.

In an alternative embodiment, the bond pads 260 and lands 280 may be co-located with the vias 250. For example, **FIG. 5** illustrates a semiconductor device 120 according to that alternate embodiment of the invention. The interconnect substrate 220 may alternately be made of a ceramic material instead of a laminate material. When the interconnect substrate is made from a ceramic material, the plurality of bond pads 260 may be co-located with the second group of vias 250 on the upper surface. The plurality of lands 280 may also be co-located with the second group of vias 250 on the lower surface. This positioning of the bond pads and lands will save space, and thus will make it possible to form an electronic package that is even smaller than the previously described embodiment.

Although the present invention has been described in conjunction with particular embodiments illustrated in the appended drawing figures, various modification may be made without departing from the spirit and scope of the invention as set forth in the appended claims. For example, an alternate material may be used for the material of interconnect

substrate 220, or bond pads 260 could be distributed in a different layout pattern on interconnect substrate 220. These and other modifications of the preferred embodiment are intended to be within the scope of the following claims.

CLAIMS

We claim:

1. An electronic package for a device, comprising:

an interconnect substrate having an upper surface and a lower surface;

a die attach pad on said upper surface for receiving a semiconductor device chip;

a heat spreader on said lower surface, said heat spreader positioned beneath said die attach pad;

a plurality of vias passing through the thickness of said interconnect substrate from said upper surface to said lower surface;

a first group of said vias positioned to intersect both said die attach pad and said heat spreader;

a second group of said vias positioned about and spaced away from said die attach pad;

a thermal conductor located in said first group to thermally interconnect said die attach pad and said heat spreader;

a plurality of bond pads positioned on said upper surface, each of said plurality of bond pads abutting one of said vias of said second group;

a plurality of lands positioned on said lower surface, each of said plurality of lands abutting one of said vias of said first group; and

an electrically conductive medium located in said second group to electrically interconnect each of said plurality of bond pads to said plurality of lands.

2. The electronic package of claim 1, wherein said interconnect substrate is constructed from an organic material.

3. The electronic package of claim 1, wherein said interconnect substrate is constructed from a ceramic material.

4. The electronic package of claim 1, wherein said plurality of bond pads are positioned in a peripheral design.

5. The electronic package of claim 1, wherein said plurality of bond pads are positioned in an array of columns and rows.

6. The electronic package of claim 1, wherein at least one of said plurality of bond pads is co-located with one of said vias of said second group.

7. The electronic package of claim 1, wherein at least one of said plurality of lands is co-located with one of said vias of said second group.

8. A semiconductor device comprising:

an interconnect substrate having an upper surface and a lower surface;

a die attach pad on said upper surface;

a heat spreader on said lower surface, said heat spreader positioned beneath said die attach pad;

a plurality of vias passing through the thickness of said interconnect substrate from said upper surface to said lower surface;

a first group of said vias positioned to intersect both said die attach pad and said heat spreader;

a second group of said vias positioned about and spaced away from said die attach pad;

a thermal conductor located in said first group to thermally interconnect said die attach pad and said heat spreader;

a plurality of bond pads positioned on said upper surface, each of said plurality of bond pads abutting one of said vias of said second group;

a plurality of lands positioned on said lower surface, each of said plurality of lands abutting one of said vias of said second group;

an electrically conductive medium located in said second group of vias to electrically interconnect each of said plurality of bond pads to said plurality of lands; and

a semiconductor device chip attached to said die attach pad and having a plurality of device electrodes on a surface thereof.

9. The semiconductor device of claim 8 further comprising electrical bonds connecting said plurality of device electrodes to said plurality of bond pads.

10. The semiconductor device of claim 8, wherein said interconnect substrate is constructed from an organic material.

11. The semiconductor device of claim 8, wherein said interconnect substrate is constructed from a ceramic material.

12. The semiconductor device of claim 8, wherein said plurality of bond pads are positioned in a peripheral design.

13. The semiconductor device of claim 8, wherein said plurality of bond pads are positioned in an array of columns and rows.

14. The semiconductor device of claim 8, wherein at least one of said plurality of bond pads is co-located with one of said vias of said second group.

15. The semiconductor device of claim 8, wherein at least one of said plurality of lands is co-located with one of said vias of said second group.

16. The semiconductor device of claim 8, wherein said electrical bonds comprise wires.

17. The semiconductor device of claim 8, further comprising an electrical connection from a surface of said semiconductor device chip to said die attach pad.

ABSTRACT OF THE DISCLOSURE

A semiconductor device is provided in the form of a chip carrier (e.g., chip/IC scale carrier for RF applications) that includes an integrated circuit chip attached to a die attach pad. The device has an interconnect substrate having an upper surface and a lower surface, with a plurality of vias passing through the thickness of the interconnect substrate from the upper surface to the lower surface. The die attach pad is located on the upper surface of the interconnect substrate, and a heat spreader is located on the lower surface of the interconnect substrate. A first group of vias is positioned to intersect both the die attach pad and the heat spreader. A second group of vias is positioned away from the die attach pad and the heat spreader. The upper surface has a plurality of bond pads that are abutting the second group of vias and the lower surface has a plurality of lands that are also abutting the second group of vias.

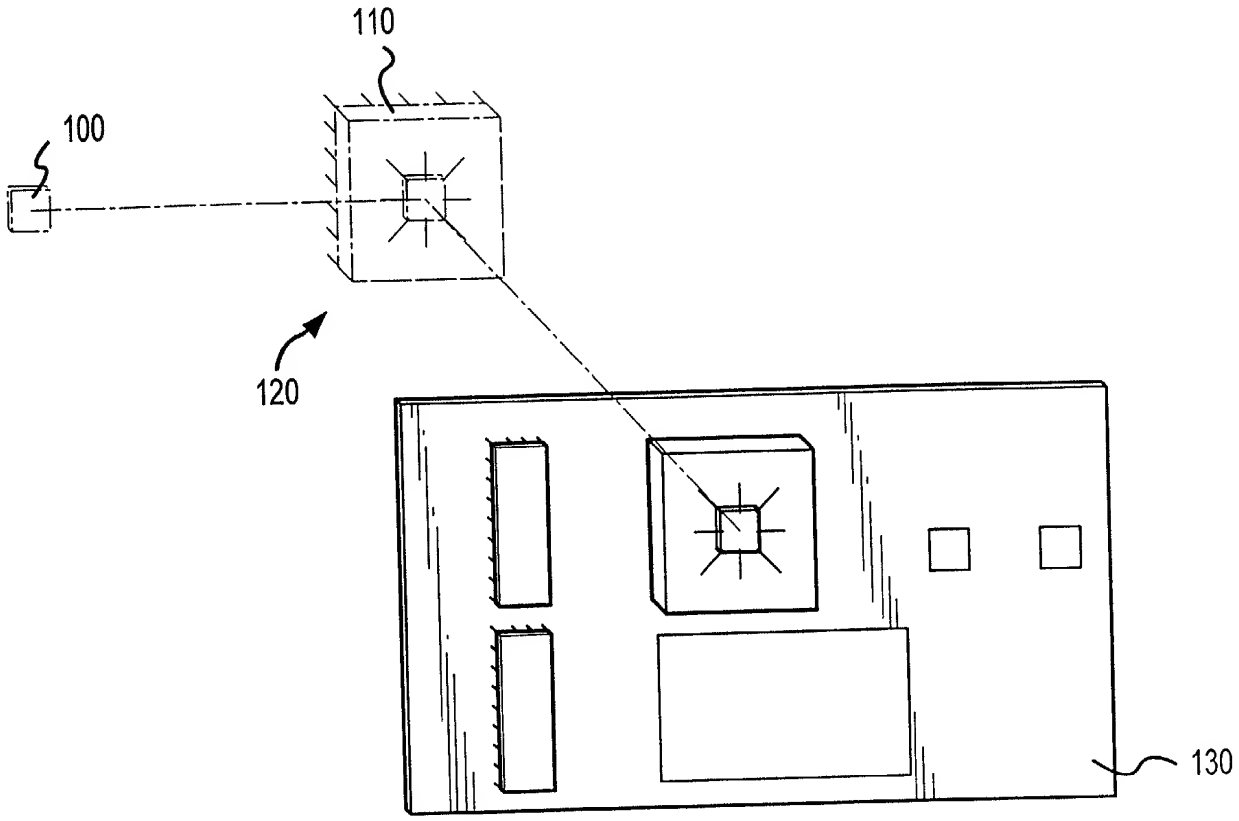
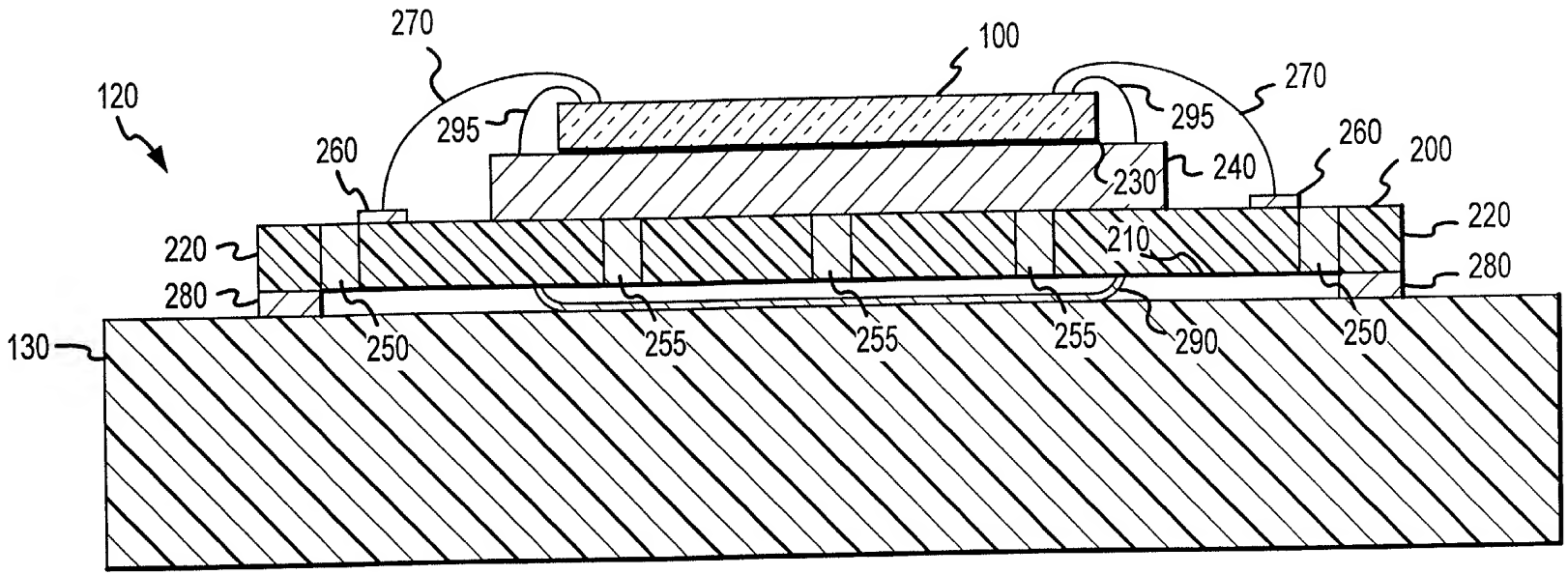


FIG.1
(PRIOR ART)


270
100
120
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295
270
260
260
200
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240
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220
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130
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290
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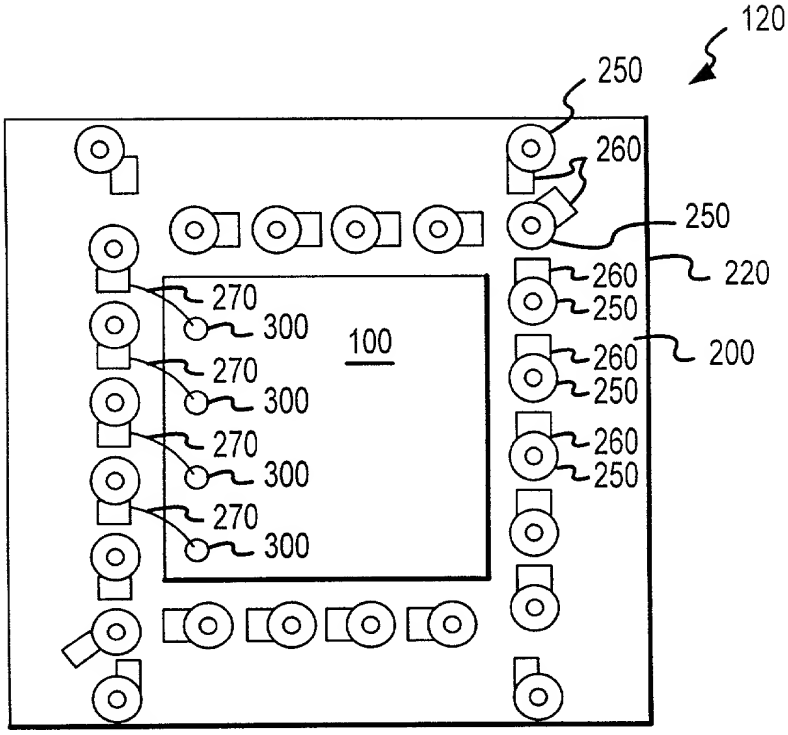
FIG.2


120
250
260
250
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260
250
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FIG.3

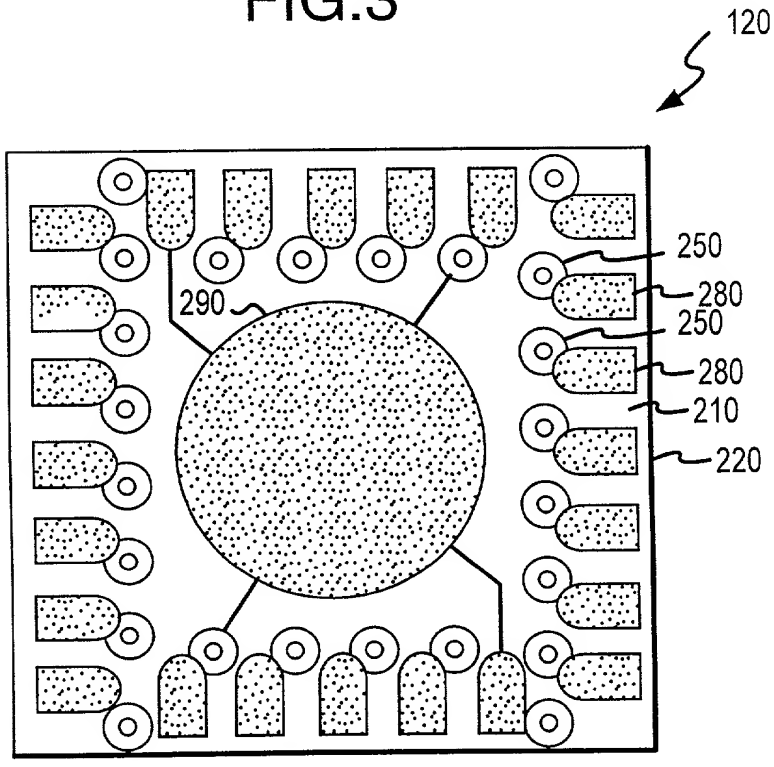
120
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FIG.4

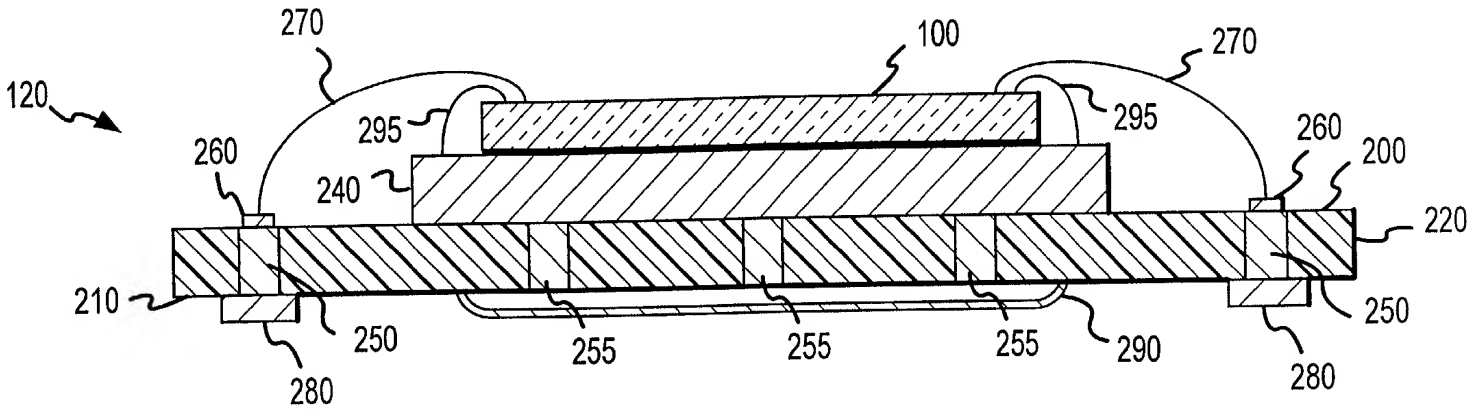
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FIG.5

Docket No.
50944.2100

Declaration For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

LEADLESS CHIP CARRIER DESIGN AND STRUCTURE

the specification of which

(check one)

☐ is attached hereto.

☒ was filed on 2/17/99 as United States Application No. or PCT International Application Number 09/252,851

and was amended on _____

(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	☐

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

(Application Serial No.)	(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, CFR Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole or first inventor **Hassan S. Hashemi**	
Sole or first inventor's signature Hassan Hashemi	Date 3/28/99
Residence **Laguna Niguel, California 92677-5507**	
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Full name of second inventor, if any	
Second inventor's signature	Date
Residence	
Citizenship	
Post Office Address	

Full name of third inventor, if any	
Third inventor's signature	Date
Residence	
Citizenship	
Post Office Address	

Full name of fourth inventor, if any	
Fourth inventor's signature	Date
Residence	
Citizenship	
Post Office Address	

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Hassan S. Hashemi

Serial No.:

Filed:

For: **Leadless Chip Carrier Design and Structure**

Continuation of co-pending application Serial No. 09/252,851, filed on 2/17/99, and Assigned to the Assignee of the present application, Conexant Systems, Inc.

REVOCATION AND POWER OF ATTORNEY

Honorable Commissioner of
Patents and Trademarks
Washington, D.C. 20231

Dear Sir/Madam:

Applicant of the above-identified patent application hereby revokes all previous powers of attorney given in this application and appoints:

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Farshad Farjami, Reg. No. 41,014
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Keith Kind, Reg. No. 42,735

with full power of substitution and revocation, to prosecute this application, to make alterations and amendments thereto, to receive communications from the Patent and Trademark Office and to

transact all business in the Patent and Trademark Office connected therewith. Please direct all communications to:

FARJAMI & FARJAMI LLP
16148 Sand Canyon
Irvine, California 92618
Telephone: (949) 784-4600

Signed this 14th day of November 2000

Daniel N. Yannuzzi, Esq.
Chief IP Counsel
Conexant Systems, Inc. (Assignee)

"EXPRESS MAIL" mailing label number EL659311809US
Date of Deposit 11-15-2000
I hereby certify that this paper is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and is addressed to the Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Sara Ansari
(Signature)
Sara Ansari
(Typed or Printed Name of Person Mailing Paper or Fee)